

**WHAT IS CLAIMED IS:**

- 1           1. A method comprising:  
2           detecting an electrical characteristic identifying a defect in a memory unit; and  
3           replacing the memory unit with an alternate memory unit, wherein the replacing is  
4                     performed during user operation of a device having the memory unit and  
5                     the alternate memory unit.
- 6           2. The method as recited in Claim 1, wherein the detecting the electrical  
7   characteristic comprises:  
8           monitoring a current during an erase attempt; and  
9           identifying the defect when the current passes a predetermined current threshold.
- 10          3. The method as recited in Claim 1, wherein the detecting the electrical  
11   characteristic comprises:  
12          monitoring a voltage during an erase attempt; and  
13          identifying the defect when the voltage passes a predetermined voltage threshold.
- 14          4. The method as recited in Claim 1, wherein the detecting the electrical  
15   characteristic comprises:  
16          monitoring a resistance during an erase attempt; and  
17          identifying the defect when the resistance passes a predetermined resistance  
18                     threshold.

19           5. The method as recited in Claim 1, wherein the monitoring is performed during  
20 an erase operation.

21           6. The method as recited in Claim 1, wherein the replacing the memory unit with  
22 the alternate memory unit comprises:

23           causing the memory unit to be un-accessible at a memory address; and

24           causing the alternate memory unit to be accessible at the memory address.

25           7. The method as recited in Claim 6, wherein the causing the alternate memory  
26 unit to be accessible comprises:

27           programming address status bits of the alternate memory unit with the memory  
28           address.

29           8. The method as recited in Claim 7, wherein the address status bits comprise  
30 non-volatile memory.

31           9. The method as recited in Claim 7, wherein the address status bits comprise  
32 programmable fuses.

33           10. The method as recited in Claim 6, wherein the causing the alternate memory  
34 unit to be accessible comprises:

35           setting a used status bit of the alternate memory unit.

36           11. The method as recited in Claim 1, wherein the memory unit is a flash memory  
37 block.

38           12. The method as recited in Claim 1, wherein the memory unit is a row of flash  
39   memory.

40           13. The method as recited in Claim 1, wherein the memory unit is a row of  
41   polymer memory.

42           14. An apparatus comprising:  
43           a plurality of accessible memory units;  
44           one or more redundant memory units;  
45           a failure detection unit coupled to the plurality of accessible memory units  
46                   configured to monitor electrical characteristics in the plurality of  
47                   accessible memory units and detect an electrical characteristic that  
48                   identifies a defect in one of the plurality of accessible memory units; and  
49           a redundant block swap unit coupled to the plurality of accessible memory units  
50                   and the one or more redundant memory units, the redundant block swap  
51                   unit configured to replace the one of the plurality of accessible memory  
52                   units with one of the one or more redundant memory units.

53           15. The apparatus as recited in Claim 14, the failure detection circuit comprising:  
54           a current detection unit to detect a current during an erase operation.

55           16. The apparatus as recited in Claim 14, the failure detection circuit comprising:  
56           a voltage detection unit to detect a voltage during an erase operation.

57           17. The apparatus as recited in Claim 14, the failure detection circuit comprising:

58 a resistance detection unit to detect a resistance during an erase operation.

59 18. The apparatus as recited in Claim 14, wherein each of the one or more

60 redundant memory units comprises:

61 a plurality of memory cells;

62 address status bits; and

63 a used status bit;

64 wherein the redundant block swap unit is configured to program the address status

65 bits and the used status bit to cause the plurality of memory cells to be

66 accessible.

67 19. The apparatus as recited in Claim 14, wherein each of the one or more

68 redundant memory units comprises a plurality of memory cells, the apparatus further

69 comprising:

70 address status bits; and

71 a used status bit;

72 wherein the redundant block swap unit is configured to program the address status

73 bits and the used status bit to cause the plurality of memory cells to be

74 accessible.

75 20. A system comprising:

76 a processor;

77 an antenna coupled to the processor; and

78 a memory device coupled to the processor, the memory device comprising:

79 a plurality of accessible memory units;

80 one or more redundant memory units;  
81 a failure detection unit coupled to the plurality of accessible memory units  
82 configured to monitor electrical characteristics in the plurality of  
83 accessible memory units and to detect a electrical characteristic that  
84 identifies a defect in one of the plurality of accessible memory units; and  
85 a redundant block swap unit coupled to the accessible memory units and  
86 the one or more redundant memory units, the redundant block swap unit  
87 configured to replace the one of the plurality of accessible memory units  
88 with one of the one or more redundant memory units.

89 21. The system as recited in Claim 20, the failure detection circuit comprising:  
90 a current detection unit to detect a current in one of the plurality of accessible  
91 memory units during an erase operation.

92 22. The system as recited in Claim 21, wherein each of the one or more redundant  
93 memory units comprises:  
94 a plurality of memory cells;  
95 address status bits; and  
96 a used status bit;  
97 wherein the redundant block swap unit is configured to program the address status  
98 bits and the used status bit to cause the plurality of memory cells to be  
99 accessible.

100           23. The system as recited in Claim 20, wherein each of the one or more redundant  
101 memory units comprises a plurality of memory cells, the memory device further  
102 comprising:

103           address status bits; and

104           a used status bit;

105           wherein the redundant block swap unit is configured to program the address status  
106           bits and the used status bit to cause the plurality of memory cells to be  
107           accessible.

108           24. An apparatus comprising:

109           a computer readable medium; and

110           instructions stored on the computer readable medium to:

111           detect an electrical characteristic that identifies a defect in a memory unit;

112           and

113           replace the memory unit with an alternate memory unit, wherein replacing

114           is performed during user operation of a device having the memory unit

115           and the alternate memory unit.

116           25. The apparatus as recited in Claim 24, wherein the instructions to detect the

117 electrical characteristic comprises instructions to:

118           monitor a current; and

119           identify a defect when the current exceeds a predetermined current threshold.

120           26. The apparatus as recited in Claim 24, wherein the instructions to detect the

121 electrical characteristic comprises instructions to:

122 monitor a voltage during an erase attempt; and  
123 identify a defect when the voltage exceeds a predetermined voltage threshold.

124 27. The apparatus as recited in Claim 24, wherein the electrical characteristic is  
125 detected during an erase operation.

126 28. The apparatus as recited in Claim 24, wherein the instructions to replace the  
127 memory unit with an alternate memory unit comprises instructions to:  
128 cause the memory unit to be un-accessible at a memory address; and  
129 cause the alternate memory unit to be accessible at the memory address.

130 29. The apparatus as recited in Claim 28, wherein the instructions to cause the  
131 alternate memory unit to be accessible comprises instructions to:  
132 program address status bits of the alternate memory unit with the memory  
133 address.

134 30. The apparatus as recited in Claim 28, wherein the instructions to cause the  
135 alternate memory unit to be accessible comprises instructions to:  
136 set a used status bit of the alternate memory unit.

137 31. The apparatus as recited in Claim 24, wherein the memory unit is a flash  
138 block.